PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-201190

(43)Date of publication of application : 18.07.2000

(51)Int.Cl. H04L 27/22

H03L 7/085

H04L 7/00

(21)Application number : 11-002491 (71)Applicant : TOSHIBA CORP
TOSHIBA AVE CO LTD

(22)Date of filing : 08.01.1999 (72)Inventor : KOMATSU SUSUMU
NISHIKAWA MASAKI

(54) CLOCK PHASE ERROR DETECTION CIRCUIT AND CLOCK PHASE ERROR DETECTION METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain a clock phase error signal satisfying clock reproducing performance at a low C/N to be used for correcting the phase of a reproduced clock in a clock reproducing circuit.

SOLUTION: The clock phase error detection circuit for obtaining a clock phase error signal for correcting the phase of a reproduced clock to be used for a circuit for reproducing a clock synchronized with a prescribed phase from a band-limited pulse code signal is provided with a decision means 2 for detecting the code pattern of a signal obtained by sampling the pulse code signal by the clock and deciding the pattern and a phase error calculation means 1 for finding out a phase error from the decided code pattern and the sampled signal by a prescribed operation.

LEGAL STATUS

[Date of request for examination]	18.02.2005
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]

[Claim 1] In the clock phase error detector which acquires the clock phase error signal for playback clock phase corrections used for the circuit which reproduces the clock which synchronized with the predetermined phase from the pulse code signal which received the band limit The judgment means which detects the sign pattern of the signal which sampled said pulse code signal with said clock, and acquired it, and carries out a pattern judging, The clock phase error detector characterized by having a phase error operation means to search for a clock phase error signal by the predetermined phase error operation from the judged sign pattern and said signal sampled and

acquired.

[Claim 2] The clock phase error detector according to claim 1 characterized by making the phase error operation in a phase error operation means calculate about four continuous symbols.

[Claim 3] A phase error operation is a clock phase error detector according to claim 1 characterized by considering as the configuration to which the multiplier of an FIR filter is switched according to said detected sign pattern while constituting a phase error operation means from an FIR filter.

[Claim 4] In the clock phase error detector which acquires the clock phase error signal for playback clock phase corrections used for the circuit which reproduces the clock which synchronized with the predetermined phase from the pulse code signal which received the band limit The judgment means which detects the sign pattern of the signal which sampled said pulse code signal with said clock, and acquired it, and carries out a pattern judging, The absolute value conversion means which carries out absolute value conversion of the signal which sampled said pulse code signal with said clock, and acquired it, The clock phase error detector characterized by having a phase error operation means to search for a clock phase error signal by the predetermined phase error operation from the signal which carried out absolute value conversion, with the sign pattern which said judgment means judged, and said absolute value conversion means.

[Claim 5] Claim 1 characterized by having the level judging circuit which detects that the pulse code signal which received the band limit is larger than the amplitude specified beforehand, and performing said phase error operation when a pulse code signal is larger than the amplitude specified beforehand, or a clock phase error detector given in 4 any 1 terms.

[Claim 6] Claim 1 characterized by making into a phase error detecting signal the value which performed said phase error operation by each of an I signal and a Q signal, and averaged each phase error result of an operation thru/or a clock phase error detector given in 5 any 1 terms.

[Claim 7] In reproducing the clock which synchronized with the predetermined phase from the pulse code signal which received the band limit While detecting the sign pattern of the signal which sampled said pulse code signal

with said clock, and acquired it, carrying out a pattern judging and searching for a phase error by the predetermined operation from this judged sign pattern and said signal sampled and acquired The phase error searched for is the clock phase error detection approach characterized by using for the phase correction of clock playback.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[The technical field which carries out an invention group] This invention relates to the clock phase error detector for acquiring the clock phase error signal used for the phase correction of the clock regenerative circuit used for the receiving set in the system which transmits a digital signal using the band-limited pulse signal, and the clock phase error detection approach.

[0001]

[Description of the Prior Art] In the system which transmits a digital signal using the band-limited pulse wave, it is made to perform a code transmission using the pulse by which roll-off spectrum plastic surgery was generally carried out. Therefore, a slight gap of the sample timing of a receiving side makes a property deteriorate rapidly.

[0002] While easy sample timing, i.e., clock playback, rectified an input signal and it extracted a clock component, he was trying to reproduce a clock through this extracted clock component conventionally to a narrow-band **** passage filter. However, in order to save transmission band width of face more and to use the small spectrum plastic surgery property of a roll-off factor in recent years, much more high performance-ization of clock playback has come to be required.

[0003] As a clock regenerative circuit which meets such a demand, the method of controlling **** shown in drawing 11 (A) is proposed. This will detect the phase control signal of a clock before and behind a zero cross point,

and will call this controlling method the zero cross controlling method here.
[0004] The zero cross controlling method is explained. (a) of drawing 11 (A) is what simplified and showed the eye pattern of a binary digital signal, and a problem does not have the condition of a signal itself on the average. And since a transmitting sign can be correctly incorporated if timing is in agreement with the phase of a signal like S1 and S2 in sample timing when sampling this binary digital signal, data are correctly reproducible.
[0005] Next, as shown in (b) of drawing 11 (A), when only Te second is in sample timing and it shifts to the location of S1' and S2', it considers what becomes. In this case, while the aperture of the eye pattern of a binary digital signal becomes narrow with W0 to W1 by having shifted from S1 to S1' Only Te second will shift and the timing which should be sampled by S2 which is a zero cross point location will also sample an input signal in the timing location of S2' in (c) of drawing 11 (A). If the sampled value (sampled value) in this sampling timing is set to e, this e will come to take a big value compared with the value which it must originally have been near the zero.
[0006] by the way -- supposing a transmitting sign changes to "+1" from "-1" before and behind a zero cross point in this case -- a sampled value -- e (- +) -- the case where took the forward value and it changes from "+1" to "-1" conversely -- a sampled value -- e (+-) -- a negative value is taken. Therefore, a gap of sample timing can be known by getting to know the transmitting sign in zero cross point order. This is the principle of zero cross control.
[0007] Thus, by the zero cross controlling method, since the value near the zero cross point is used, it is not based on the amplitude of an eye pattern, but there is the description which operates. However, since e (- +) and e (+-) may not become zero and a control signal occurs at this time even if the eye pattern is carrying out the wave as shown in drawing 12 in fact and the clock phase synchronizes, the problem which says that there are many jitters remains.
[0008] On the other hand, the method of controlling **** shown in drawing 11 (B) is also developed. This is a method which detects the phase control signal of a clock before and after the eye pattern convergence point, and this will be called the eye convergent point controlling method here. That is, the eye

convergent point controlling method is the controlling method like a degree. (a) of drawing 11 (B) shows the eye pattern of a binary digital signal, and T-1 [of drawing 11 (B)] of (b), and T0 and T1 show the optimal clock phase. Although sampled by reference level L1, L2, and L3 with the 2-bit A/D converter in this example, the example using a multiple-value A/D converter is considered. If the clock phase has +deltat Shifted when a transmitting sign changes with a-1, and B0 and C1, a sampled value will turn into a bigger value than reference level L1, and if it has -deltat Shifted, a sampled value will turn into a value smaller than reference level L1.

[0009] therefore, the difference of the transmitting sign before and behind a control point, and the reference level in a control point -- a gap of sample timing is detectable with a value.

[0010] Thus, since the value near the eye convergence point is used, there are few jitters at the time of phase simulation, and they can be managed with the eye convergent point controlling method. however -- a case so that the amplitude of an eye pattern may change -- difference with reference level -- in order that a value may not show a gap of sample timing correctly, it has the problem referred to as being unable to perform control of a clock phase.

[0011] Then, the **** technique shown in Japanese Patent Application No. No. (refer to JP,5-327681,A) 126041 [four to] is developed as a clock regenerative circuit which solved these problems and attained high performance-ization of clock playback.

[0012] This is ******** shown in drawing 13 , and it will be called the clock phase error detection controlling method. This clock phase error detection controlling method is explained. Drawing 13 (a) shows the eye pattern and shows the case where the sampled values of the eye convergence point are "L0" and "-L0." a now and clock phase -- "+deltat" -- the case where it has shifted is considered. Supposing a transmitting sign changes with "A1" and "B-2" in this condition, in the sampled value of "A1", the sampled value of "-(L0-deltal)" and "B-2" will become "(L0+deltal)." Here, when the absolute value of each sampled value is compared, it is |L0+deltal|-|-(L0-deltal)|=2deltal>0, and the sampled value of "B-2" is larger in an absolute value.

[0013] Moreover, when a transmitting sign changes with "B1" and "A2", in the

sampled value of "B1", the sampled value of "(L0-deltal)" and "A2" becomes "-(L0+deltal)." Here, when the absolute value of each sampled value is compared, it is |-(L0+deltal) |-|(L0-deltal) |=2deltal>0, and it turns out in an absolute value that the sampled value of "A2" is larger.

[0014] That is, it turns out that it is said that the next value of the absolute value of two samples which continue when the clock phase is behind (clock phase "+deltat") is larger, and the next value of the absolute value of two continuous samples is smaller when the clock phase is progressing similarly (clock phase "-deltat").

[0015] Phase contrast can be acquired if this searches for the amplitude difference between continuous 2 samples.

[0016] namely, in the case where the phase error in the clock phase error detection controlling method is detectable As the principle explained by drawing 13 is shown in drawing 14 which is drawing which expressed typically If the sample point **t Shifted when the input configuration which is a generating pattern of four symbols with which the inputted pulse code continues took the location of a symbol "A0", "A1", "B-2", and "B3", a phase error can be searched for as "2deltal."

[0017] Moreover, contrary to this, although it is an example when a phase error is undetectable, a phase error cannot be set to "O" and drawing 15 cannot search for it in this example, supposing the sample point **t Shifts, when the input configuration of the input signal which is the generating pattern of four symbols with which the inputted pulse code continues takes the location of a symbol "B0", "A1", "B-2", and "A3."

[0018] Therefore, between [from just before the sample timing T1] immediately after the following sample timing T2, it will be restricted that a phase error is detectable by the clock phase error detection controlling method of a Japanese-Patent-Application-No. No. 126041 [four to] indication, when an input signal increases [monotone-] or decreases [monotone-].

[0019] A signal is a case like drawing 14 and this is a total of two kinds, the case where the input configuration of four continuous symbols takes the location of "A0", "A1", "B-2", and "B3", and the case where the location of "B0", "B1", "A2", and "A3" is taken. Since the number of the input configuration

variations of four continuous symbols is 16, "one eighth of probabilities" cannot but detect a phase error by the clock phase error detection controlling method concerned, and it can search for a phase error from input data only by the low probability which it says is "one eighth."

[0020] Thus, since the probability which can carry out phase error detection was low, the clock playback with low [C/N] was inadequate.

[0021]

[Problem(s) to be Solved by the Invention] In the system which transmits a digital signal using the band-limited pulse wave, in order to save transmission band width of face, it comes to use the small spectrum plastic surgery property of a roll-off factor, therefore much more high performance-ization of clock playback has come to be required. And the **** technique shown in Japanese Patent Application No. No. (refer to JP,5-327681,A) 126041 [four to] is developed as a clock regenerative circuit which meets such a demand.

[0022] However, between [from just before sample timing] immediately after the following sample timing, it will be restricted that a phase error is detectable with this technique, when an input signal increases [monotone-] or decreases [monotone-].

[0023] Although this cannot but be two kinds as an input configuration, since it is 16 kinds as an input configuration of four continuous symbols, "one eighth of probabilities" cannot but detect a phase error to input data by the clock phase error detection controlling method concerned, and a phase error can be searched for only by the low probability which it says is "one eighth."

[0024] Thus, by the conventional approach, since the probability which can carry out phase error detection was low, there was a problem that clock reproducibility ability low [C/N] was inadequate.

[0025] Then, the place made into the purpose of this invention is to offer the clock phase error detector and the clock phase error detection approach of being able to carry out phase error detection in a high probability, being able to acquire the clock phase error signal used for the phase correction of a clock regenerative circuit, and having enabled it to satisfy clock reproducibility ability low [C/N].

[0026]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is constituted as follows. Namely, it sets to the clock phase error detector which acquires the clock phase error signal for playback clock phase corrections used for the circuit which reproduces the clock which synchronized with the predetermined phase from the pulse code signal which received the band limit. The judgment means which detects the sign pattern of the signal which sampled said pulse code signal with said clock, and acquired it, and carries out a pattern judging, It is characterized by having a phase error operation means to search for a clock phase error signal by the predetermined phase error operation from the judged sign pattern and said signal sampled and acquired. Moreover, while constituting especially a phase error operation means from an FIR filter, it is characterized by considering a phase error operation as the configuration which switches the multiplier of an FIR filter according to said detected sign pattern.

[0027] In reproducing the clock which synchronized with the predetermined phase from the pulse code signal which received the band limit, this invention detects the sign pattern of the signal which sampled said pulse code signal with said clock, and acquired it, carries out a pattern judging, and searches for a phase error by the predetermined operation from this judged sign pattern and said signal sampled and acquired. And the phase error searched for is used for the phase correction of clock playback.

[0028] Moreover, if an FIR filter is used, things can be carried out, and in all continuous sign patterns, phase error detection can be carried out now by the thing which constitute a phase error operation means easily and for which a filter factor is changed into input configuration correspondence, and an error operation can amend a phase shift promptly, when a gap arises in the clock phase in the case of clock playback.

[0029] In the circuit which reproduces the clock with which especially this invention synchronized with the predetermined phase from the pulse code signal which received the band limit By detecting the sign pattern of the signal sampled with said clock, and calculating a phase error according to said detected sign pattern In all continuous sign patterns, since phase error detection can be carried out now In many case, phase error detection is

possible, therefore the probability for a phase error to be detectable from an input signal can be raised, and clock reproducibility ability low [C/N (carrier noise ratio)] can be improved.

[0030] Therefore, according to this invention, the clock playback with which are satisfied of clock reproducibility ability low [C/N] is attained.

[0031]

[The mode of implementation of invention] Hereafter, the example of this invention is explained with reference to a drawing.

[0032] (Example 1) The block diagram of one example of the clock phase error detector which is this invention is shown in drawing 1 . drawing -- setting -- 1 -- a phase error arithmetic circuit and 2 -- for an effective judging circuit and 5, as for an input terminal and 7, a hold circuit and 6 are [a pattern judging circuit and 3 / a level judging circuit and 4 / a threshold input terminal and 8] output terminals.

[0033] The input signal which sampled and acquired the received pulse code signal to playback clock timing is inputted into an input terminal 6 among these. In addition, a pulse code signal here is a pulse code signal which received the band limit. The phase error arithmetic circuit 1 performs an error operation according to the sign pattern of this input signal, and gives the error data which are the result of an operation to a hold circuit 5.

[0034] The pattern judging circuit 2 is for judging the sign pattern of an input signal inputted from the input terminal 6, and the level judging circuit 3 is for judging the level of the input signal inputted from the input terminal 6, and it detects that the level of the input signal concerned is larger than the threshold supplied from the threshold input terminal 7.

[0035] If the pattern judging result by the pattern judging circuit 2 and the level judging result by the level judging circuit 3 judge and are satisfied, the effective judging circuit 4 whether it is satisfied with coincidence Validity, It is what carries out an "invalid" judgment if not satisfied. A hold circuit 5 The error data which the phase error arithmetic circuit 1 outputs when the judgment result of the effective judging circuit 4 is "effective" as it is Through, This is outputted as a clock phase error signal, and if the judgment result of the effective judging circuit 4 is "invalid", the error signal of the phase error

arithmetic circuit 1 in front of that will be held by making this into a hold signal, and it will output as a clock phase error signal. The clock phase error signal from a hold circuit 5 is outputted to an output terminal 8.

[0036] The input signal which such this equipment of a configuration sampled the pulse code signal to playback clock timing, and was acquired is inputted from an input terminal 6. This input signal branches to the phase error arithmetic circuit 1, the level judging circuit 3, and the pattern judging circuit 2.

[0037] First, it detects that the level judging circuit 3 has input signal level larger than the threshold supplied from the threshold input terminal 7. Since it is a problem whether this threshold is too large or it is too small and, according to the purpose, the optimal value will be chosen experientially, but as standardly shown in drawing 2 , for example, "+L0 / 2", and -L0 / "2" extent which are about 50% of value of input signal level "+L0" and "-L0" are good.

[0038] In addition, since a phase error is calculated using "4 Sample" so that it may mention later in this example, in the level judging circuit 3, "4 Sample" which continues also in this level judging judges to coincidence that it is larger than a threshold. A judgment result is supplied to the effective judging circuit 4.

[0039] Next, the pattern judging circuit 2 judges the sign pattern of the above "4 Sample." And the judgment result is supplied also to the effective judging circuit 4, in order to judge whether it is a pattern effective in an error operation, while the phase error arithmetic circuit 1 is supplied as a multiplier change-over signal for a phase error operation.

[0040] The effective judging circuit 4 judges whether it is satisfied with coincidence of the pattern judging result and the level judging result. That is, in accordance with the pattern with which the sign pattern of continuous "4 Sample" can perform a phase error operation, further, when larger than the threshold as which the signal amplitude was specified beforehand, it judges with it being "effective". When not satisfied with coincidence of two above-mentioned judgments, it judges with it being "invalid", and the judgment signal [""] concerned is supplied to a hold circuit 5 as a hold signal.

[0041] On the other hand, the phase error arithmetic circuit 1 performs an error operation according to the sign pattern of an input signal, and supplies the error data which are the result of an operation to a hold circuit 5. A hold

circuit 5 is outputted to an output terminal 8 by making into a clock phase error signal the error data supplied from the phase error arithmetic circuit 1. However, when the hold signal is supplied from the effective judging circuit 4, the clock phase error signal in front of that is held, and it is judged that the error data supplied from the phase error arithmetic circuit 1 are "invalid".

[0042] A hold circuit 5 the error data which the phase error arithmetic circuit 1 outputs when the judgment result of the effective judging circuit 4 is "effective" as it is Therefore, through, It outputs to an output terminal 8 by making this into a clock phase error signal, if the judgment result of the effective judging circuit 4 is "invalid", the error signal of the phase error arithmetic circuit 1 in front of that will be held by making this into a hold signal, and it will output to an output terminal 8 as a clock phase error signal.

<The configuration of a phase error arithmetic circuit>, next the concrete example of the phase error arithmetic circuit 1 are explained using drawing 3 . As shown in drawing 3 , the phase error arithmetic circuit 1 is realized by the FIR filter which consists of adders 209 adding each output of the adjustable coefficient multiplier 205,206,207,208 to which the delay output from the delay element 201,202,203,204 and each [these] delay element 201,202,203,204 of serial connection is supplied, and these adjustable coefficient multiplier 205,206,207,208.

[0043] A sampling signal is supplied from the sampling signal input terminal 210. The sampling signal supplied from this sampling signal input terminal 210 is supplied in order of a delay element 201, a delay element 202, a delay element 203, and a delay element 204. After the signal delayed, respectively is amplified among the coefficient-of-variable-capacitance machines 205,206,207,208 according to each multiplier with each corresponding coefficient-of-variable-capacitance vessel 205,206,207,208, it is added with an adder 209, an error operation is completed, and it is outputted to a hold circuit 5 as error data from an output terminal 212.

[0044] The multiplier change-over signal is supplied to the input terminal 211 from the pattern judging circuit 2, the coefficient C 3 of the coefficient-of-variable-capacitance machine 205,206,207,208, and C2, C1 and C0 are controlled according to a multiplier change-over signal, and a filter shape is

switched.

[0045] The approach of an error operation is explained with reference to <approach of error operation> drawing 4 . (a) in drawing 4 is a sampling signal supplied from an input terminal 210. The sign patterns of the signal shown here are "A0" (=-L0), "A1" (=-L0), "B-2" (=+L0)" in drawing 6 , and "A3" (=+L0). As shown in drawing 4 (b), to this sign pattern the multiplier of the adjustable coefficient multiplier (C0) 205, the adjustable coefficient multiplier (C1) 206, the adjustable coefficient multiplier (C2) 207, and the adjustable coefficient multiplier (C3) 208 If a multiplier setup is carried out at order with "-1", "+2", "0", and "-1", respectively and an FIR filter is constituted when the FIR filter output, i.e., the error result of an operation, does not have clock delay at the time of 1 clock ****** of "-3L0" clock delay, it becomes ** like drawing 4 (c) from which "0" and clock progress are set to "+3L0" at the time of 1 clock ******.

[0046] The multiplier of drawing 4 (b) In addition, "C0=-1", "C 1= 2", "C 2= 0", The case (a sampled value is "L0" or "-L0") where each sampled value takes the value which shows "C3=-1" and is shown in drawing 4 (a) is in the condition of a phase error "zero", and the value at the time of the time of day t of drawing 4 (c) being t= 0 is the error result of an operation.

[0047] Here, a clock phase error considers 1 clock **** case. Then, since time of day t is in the condition of "t= +1" when the filter output at this time is set to "-3L0" since the time of day t of 1 clock delay ****** case is in the condition of "t=-1" so that drawing 4 (c) may show, and it is by 1 clock ****, it turns out that the filter output at this time is set to "+3L0."

[0048] Although the above is considered with the value by which the input signal was sampled, when the continuous ringing of the band-limited pulse code is inputted, a result like drawing 4 (d) of having continued is obtained. This means that a filter output changes near the time of day t= 0 shown in this drawing 4 (d), when a timing gap of a sampling, i.e., a sampling phase error, arises.

[0049] Thus, in the phase error arithmetic circuit 1 in this example, the filter output which constitutes the phase error arithmetic circuit 1 concerned takes a forward value, when the clock phase is behind, and when it is behind, it takes

a negative value. Moreover, since it becomes zero when there is no phase error, a filter output, i.e., the output of the phase error arithmetic circuit 1, will express a phase error.

[0050] Drawing 5 shows the filter factor in which the error operation in each input configuration is possible. Although it changes with symbol values before and behind "4 Symbol", according to the phase error arithmetic circuit 1 of a configuration with the filter of drawing 3 , the filter output which the time of phase lag to the time of a phase lead lag network increases to continuation can be altogether obtained like drawing 4 (d).

[0051] And according to the phase error arithmetic circuit 1 of a configuration with the filter of drawing 3 , as shown in drawing 5 among "16 Patterns" which the sign pattern of "4 Symbol" has, an error operation is possible about "16 Pattern."

[0052] Namely, as the principle explained by drawing 4 is shown in drawing 6 which is drawing which expressed typically in the case where a phase error is detectable When an input configuration takes arrangement of [1 "A0"], "A1", "B-2", and "B3", When taking arrangement of [2 "B0"], "B1", "A2", and "A3", When taking arrangement of [3 "A0"], "A1", "B-2", and "A3" and taking arrangement of [4 "B0"], "B1", "A2", and "B3", When taking arrangement of [5 "A0"], "B1", "A2", and "A3" and taking arrangement of [6 "B0"], "A1", "B-2", and "B3", When taking arrangement of [7 "A0"], "A1", "A2", and "B3" and taking arrangement of [8 "B0"], "B1", "B-2", and "A3", When taking arrangement of [9 "B0"], "A1", "A2", and "A3", When taking arrangement of [10 "A0"], "B1", "B-2", and "B3", When taking arrangement of [11 "A0"], "B1", "B-2", and "A3", When taking arrangement of [12 "B0"], "A1", "A2", and "B3", When taking arrangement of [13 "A0"], "B1", "A2", and "B3", and taking arrangement of [14 "B0"], "A1", "B-2", and "A3", in a total of 14 patterns of **, a phase error can be searched for according to the phase shift of the sample point.

[0053] Moreover, contrary to this, although drawing 7 is the example which was not able to detect a phase error conventionally In this example, when input configurations were "B0", "B1", "B-2", and "B3", and when it was "A0", "A1", "A2", and "A3", even if the sample point shifted, a phase error was not

able to be set to "O" and it was able to ask for neither.

[0054] However, this can also detect a phase error in this invention.

[0055] That is, as shown in drawing 5 , when the variation of the sign pattern of "4 Symbol" takes arrangement of [15 "B0"], "B1", "B-2", and "B3", the time of taking arrangement of [16 "A0"], "A1", "A2", and "A3" -- including -- all -- coming out -- "16 patterns" -- being certain, although it divides and comes out Error operations including a total of two patterns of the pattern which takes arrangement of the pattern which takes arrangement of "A0", "A1", "A2", and "A3" from which such a sign does not change and "B0", "B1", "B-2", and "B3" are possible. This means that phase error detection precision went up rather than the conventional error operation approach.

[0056] In addition, in order to prevent degradation of the phase error detection precision by the pattern judging mistake at the time of low C / N, when the amplitude of a sampling signal is smaller than the threshold specified beforehand, a hold circuit 5 operates so that the last phase error signal may be held without using the error result of an operation.

[0057] And using the phase error signal acquired through this hold circuit 5 as a phase control signal, phase control of a clock regenerative circuit is carried out and the phase shift of a playback clock is corrected to the phase control signal correspondence concerned.

[0058] In this example, if the sample point shifts about a total of 16 patterns including no less than two patterns in case the appearance gestalt of four continuous symbols does not have the variation of sign, all can search for this phase error, can carry out phase control of a clock regenerative circuit, using the phase error signal acquired as a phase control signal, and can correct the phase shift of a playback clock to the phase control signal correspondence concerned. Therefore, since a phase error signal can be acquired about all 16 patterns in 16 patterns which are all the variations of arrangement of a symbol, when it increases by leaps and bounds and the phase shift of a clock regenerative circuit generates phase error detection precision rather than the conventional error operation approach, operation of correction control of a phase shift is attained promptly.

[0059] Therefore, phase error detection can be carried out in a high probability,

and the clock phase error detector with which can acquire the clock phase error signal used for the phase correction of a clock regenerative circuit, and enabled it to be satisfied of clock reproducibility ability low [C/N] is obtained.

[0060] Next, another example of this invention is explained as an example 2.

[0061] (Example 2) Drawing 8 is another example of this invention. In drawing 8 , 1 is a phase error arithmetic circuit and an absolute-value circuit with which a pattern judging circuit and 3 obtain a level judging circuit, and, as for 502, 4 obtains the absolute value of an effective judging circuit and the input signal into which an input terminal and 7 are inputted into for a hold circuit and 6, and an output terminal and 501 are inputted [5] for a threshold input terminal and 8 from an input terminal 6.

[0062] the point of having given the input signal which formed the absolute-value circuit 501 in the preceding paragraph of the phase error arithmetic circuit 1 in this example, and was inputted into the input terminal 6 to the phase error arithmetic circuit 1 through this absolute-value circuit 501 -- and Although the point to which that to which the level judging circuit 3 also absolute-value-ized the input signal inputted from the input terminal 6 with the absolute-value circuit 501 is given to, and it was made to carry out a level judging of this differs from an example 1, other configurations are not fundamentally different from an example 1. However, in this example, when the input signal sampled to playback clock timing is inputted into an input terminal 6, the pattern judging circuit 502 will carry out a pattern judging about this.

[0063] Moreover, with an absolute-value circuit 501, the phase error arithmetic circuit 1 performs an error operation according to the sign pattern of this input signal, using as an input that by which the sign pattern of an input signal was absolute-value-ized, and gives the error data which are the result of an operation to a hold circuit 5.

[0064] In addition, the level judging circuit 3 is for judging level, although the input signal inputted from the input terminal 6 was absolute-value-ized with the absolute-value circuit 501. It is what detects that the level of the input signal concerned is larger than the threshold supplied from the threshold input terminal 7. The effective judging circuit 4 If satisfied [judge and], whether it is

satisfied with coincidence of the pattern judging result by the pattern judging circuit 502, and the level judging result by the level judging circuit 3 Validity, It is what carries out an "invalid" judgment if not satisfied. A hold circuit 5 The error data which the phase error arithmetic circuit 1 outputs when the judgment result of the effective judging circuit 4 is "effective" as it is Through, This is outputted as a clock phase error signal, and if the judgment result of the effective judging circuit 4 is "invalid", the error signal of the phase error arithmetic circuit 1 in front of that will be held by making this into a hold signal, and it will output as a clock phase error signal. The clock phase error signal from a hold circuit 5 is outputted to an output terminal 8.

[0065] The input signal with which such this equipment of a configuration was sampled to playback clock timing is inputted from an input terminal 6. This input signal branches to an absolute-value circuit 501 and the pattern judging circuit 502.

[0066] Then, after an absolute-value circuit 501 performs absolute value conversion of an input signal, it is supplied to the phase error arithmetic circuit 1 and the level judging circuit 3. Therefore, that by which the sign pattern of an input signal was absolute-value-ized will be given to the phase error arithmetic circuit 1 and the level judging circuit 3.

[0067] And it detects whether the level judging circuit 3 has the absolute value of input signal level larger than the threshold supplied from the threshold input terminal 7. Here, since a phase error is calculated using "4 Sample", "4 Sample" which continues also in this level judging judges to coincidence that it is larger than a threshold. A judgment result is supplied to the effective judging circuit 4.

[0068] Moreover, the pattern judging circuit 502 judges the sign pattern of the above "4 Sample" about the input signal from an input terminal 6. And the judgment result is supplied also to the effective judging circuit 4, in order to judge whether it is a pattern effective in an error operation, while supplying the phase error arithmetic circuit 1 as a multiplier change-over signal for a phase error operation.

[0069] The effective judging circuit 4 judges whether it is satisfied with coincidence of the pattern judging result and the level judging result. That is,

in accordance with the pattern with which the sign pattern of continuous "4 Sample" can perform a phase error operation, further, when larger than the threshold as which the signal amplitude was specified beforehand, it judges with it being "effective". When not satisfied with coincidence of two above-mentioned judgments, it judges with it being "invalid", and the judgment signal [""] concerned is supplied to a hold circuit 5 as a hold signal.

[0070] On the other hand, the phase error arithmetic circuit 1 performs an error operation according to the sign pattern of the absolute-value-ized input signal, and supplies the error data which are the result of an operation to a hold circuit 5. A hold circuit 5 is outputted to an output terminal 8 by making into a clock phase error signal the error data supplied from the phase error arithmetic circuit 1. However, when the hold signal is supplied from the effective judging circuit 4, the clock phase error signal in front of that is held, and it is judged that the error data supplied from the phase error arithmetic circuit 1 are "invalid".

[0071] A hold circuit 5 the error data which the phase error arithmetic circuit 1 outputs when the judgment result of the effective judging circuit 4 is "effective" as it is Therefore, through, It outputs to an output terminal 8 by making this into a clock phase error signal, if the judgment result of the effective judging circuit 4 is "invalid", the error signal of the phase error arithmetic circuit 1 in front of that will be held by making this into a hold signal, and it will output to an output terminal 8 as a clock phase error signal.

[0072] And using this phase error signal as a clock phase error signal, phase control of a part for this signal correspondence and a clock regenerative circuit is carried out, and the phase shift of a playback clock is corrected to the phase control signal correspondence concerned.

[0073] Thus, this example is characterized by carrying out an error operation to the input signal which performed absolute value conversion.

[0074] namely, -- if the difference from said example 1 is explained in this example using drawing 9 -- a degree -- like -- it comes out. What is necessary is just to transform the sign of the coefficient-of-variable-capacitance machine along which the symbol from which the sign was changed by absolute value conversion, i.e., a signal with a negative value, passes, in order to obtain the

same error result of an operation as said example to the input signal which performed absolute value conversion. Decision attaches this easily from the configuration of an FIR filter.

[0075] Then, if code translation of the 16 variation ****** filter coefficient of drawing 5 is carried out when a corresponding input configuration is a negative value, and a variation is reduced, a filter coefficient will serve as a variation like drawing 9 . Here, when it takes notice of the variation of a filter coefficient, it turns out that a filter factor is seven kinds, "A", "A'", "B", "B'", "C", "C'", and "D."

[0076] That is, the number of filter factors can be reduced by carrying out absolute value conversion of the input signal.

[0077] This means the simplification of circuitry, i.e., reduction of circuit scales, and easy-ization of control. Moreover, the variation "A" of a filter coefficient, "A'", "B", "B'", and "C" and "C'" are only understood that the sign of a multiplier is reversed, respectively. For example, if an error operation is performed with the filter coefficient of a variation "A" and the sign of the result of an operation is reversed by the way, the completely same result as having performed [whose filter coefficient of a variation "A'" is the need] the error operation using the filter factor of a variation "A'" will be obtained.

[0078] By doing in this way, if a required filter coefficient is four kinds, and ends and the filter factor of four kinds of this variation is prepared, it is understood that an error operation is possible.

[0079] And using the phase error signal acquired through a hold circuit 5 as a phase control signal, phase control of a clock regenerative circuit is carried out and the phase shift of a playback clock is corrected to the phase control signal correspondence concerned.

[0080] It sets to all a total of 16 patterns including two patterns in case the appearance gestalt of four continuous symbols does not have the variation of sign at this example. If the sample point shifts, all can search for this phase error. Using the phase error signal (clock phase error signal) acquired as a clock phase control signal, clock phase control of a clock regenerative circuit can be carried out, and the phase shift of a playback clock can be corrected to the phase control signal correspondence concerned. Therefore, since a phase

error signal can be acquired about all 16 patterns in 16 patterns which are all the variations of arrangement of a symbol, when it increases by leaps and bounds and the phase shift of a clock regenerative circuit generates phase error detection precision rather than the conventional error operation approach, operation of correction control of a phase shift is attained promptly.

[0081] And the number of filter factors used with the filter which constitutes a phase error arithmetic circuit from this example by carrying out absolute value conversion of the input signal can be reduced from 16 patterns in the case where absolute value conversion is not carried out, to seven patterns of that one half, and further 4 patterns. Therefore, the simplification of circuitry, i.e., reduction of circuit scales, and easy-ization of control become being able to plan.

[0082] Therefore, phase error detection can be carried out in a high probability, and the clock phase error detector with which can acquire the clock phase error signal used for the phase correction of a clock regenerative circuit, and enabled it to be satisfied of clock reproducibility ability low [C/N] is obtained.

[0083] (Example 3) Drawing 10 is the case of the receiver which restores to a quadrature amplitude modulation, for example, a QPSK modulating signal, by the application of the above-mentioned example.

[0084] Since a QPSK modulating signal consists of an I signal and a Q signal, an error operation is performed by each of an I signal and a Q signal, and it considers as the configuration which outputs a phase error signal from each effective judging result. It is the form where the configuration shown in drawing 8 was fundamentally prepared the object for I signals, and for Q signals by two lines. The object for I signal networks It consists of an absolute-value circuit 501, the phase error arithmetic circuit 1, a pattern judging circuit 502, a level judging circuit 3, and an effective judging circuit 4. The object for Q signal networks It consists of an absolute-value circuit 706, the phase error arithmetic circuit 701, a pattern judging circuit 702, a level judging circuit 703, and an effective judging circuit 704.

[0085] A circuit 501 and the phase error arithmetic circuit 701 of the level judging circuit 3 and the effective judging circuit 704 of the pattern judging circuit 502 and the level judging circuit 703 are [an absolute-value circuit 706

/ the phase error arithmetic circuit 1 and the pattern judging circuit 702] here, the same as the effective judging circuit 4 absolutely.

[0086] The average circuit 707, a selector 708, a delay circuit 709, and IQ judging circuit 710 are further added to this configuration, and it is constituted. The average circuit 707 takes the average of the error data from an I signal, and the error data from a Q signal, and gives it to a selector 708 in quest of these averages in response to the output of the phase error arithmetic circuit 1 and the phase error arithmetic circuit 701.

[0087] Moreover, the output of the phase error arithmetic circuit 1 and the output of the phase error arithmetic circuit 701, the output of the average circuit 707, and the output of a delay circuit 709 are inputted, and a selector 708 chooses and outputs these either to selection-signal correspondence of IQ judging circuit 710.

[0088] When both networks are "effective", IQ judging circuit 710 based on the effective judging result of the I signal network outputted from the effective judging circuit 4, and the effective judging result from the Q signal network outputted from the effective judging circuit 704 moreover, the output of the average circuit 707 and -- case only the effective judging result of an I signal network is "effective" -- the output of the phase error arithmetic circuit 1 -- and When only the effective judging result of a Q signal network is "effective", when the both sides of the output of the phase error arithmetic circuit 701, an I signal network, and a Q signal network are "invalid", they generate a selection signal and give a selector 708 so that the output of a delay circuit 709 may be chosen.

[0089] Moreover, one clock of delay circuits 709 is delayed, they output the output of a selector 708 to a selector 708 again, and acquire the phase error signal which carried out 1 clock delay. Therefore, although the hold circuit is not given in the example 3, a role of the hold circuit in an example 2 is played by the delay circuit 709 and the selector 708.

[0090] The Q signal by which the I signal with which such this equipment of a configuration was sampled to playback clock timing was inputted from the input terminal 6, and was sampled to playback clock timing is inputted from an input terminal 705.

[0091] And this inputted I signal branches to an absolute-value circuit 501 and the pattern judging circuit 502, and the inputted Q signal branches to an absolute-value circuit 706 and the pattern judging circuit 702.

[0092] Then, after the absolute-value circuit 501 of an I signal network into which the I signal was inputted performs absolute value conversion of the input signal concerned, it is supplied to the phase error arithmetic circuit 1 and the level judging circuit 3. Therefore, that by which the sign pattern of an input signal was absolute-value-ized will be given to the phase error arithmetic circuit 1 and the level judging circuit 3.

[0093] And it detects whether the level judging circuit 3 has the absolute value of input signal level larger than the threshold supplied from the threshold input terminal 7. Here, since a phase error is calculated using "4 Sample", "4 Sample" which continues also in this level judging judges to coincidence that it is larger than a threshold. A judgment result is supplied to the effective judging circuit 4.

[0094] Moreover, the pattern judging circuit 502 judges the sign pattern of the above "4 Sample" about the I signal which is a direct input signal from an input terminal 6. And the judgment result is supplied also to the effective judging circuit 4, in order to judge whether it is a pattern effective in an error operation, while supplying the phase error arithmetic circuit 1 as a multiplier change-over signal for a phase error operation.

[0095] The effective judging circuit 4 judges whether it is satisfied with coincidence of the pattern judging result and the level judging result. That is, in accordance with the pattern with which the sign pattern of continuous "4 Sample" can perform a phase error operation, further, when larger than the threshold as which the signal amplitude was specified beforehand, it judges with it being "effective". When not satisfied with coincidence of two above-mentioned judgments, it judges with it being "invalid", and the judgment signal [""] concerned is supplied to IQ judging circuit 710 as a hold signal.

[0096] On the other hand, the phase error arithmetic circuit 1 performs an error operation according to the sign pattern of the absolute-value-ized input signal, and supplies I error data (error result of an operation of an I signal network) which are the result of an operation to the average circuit 707 and a

selector 708. And if the average circuit 707 has Q error data (error result of an operation of a Q signal network) from the phase error arithmetic circuit 701 for Q signal networks, it will output this and the averaged result and will give it to a selector 708.

[0097] On the other hand, after the absolute-value circuit 706 of a Q signal network into which the Q signal was inputted performs absolute value conversion of the input signal concerned, it is supplied to the phase error arithmetic circuit 701 and the level judging circuit 703. Therefore, that by which the sign pattern of an input signal was absolute-value-ized will be given to the phase error arithmetic circuit 701 and the level judging circuit 703.

[0098] And it detects whether the level judging circuit 703 has the absolute value of input signal level larger than the threshold supplied from the threshold input terminal 7. Here, since a phase error is calculated using "4 Sample", it continues also in this level judging. "4 Sample" judges to coincidence that it is larger than a threshold. A judgment result is supplied to the effective judging circuit 4.

[0099] Moreover, the pattern judging circuit 702 judges the sign pattern of the above "4 Sample" about the Q signal which is a direct input signal from an input terminal 705. And the judgment result is supplied also to the effective judging circuit 704, in order to judge whether it is a pattern effective in an error operation, while supplying the phase error arithmetic circuit 701 as a multiplier change-over signal for a phase error operation.

[0100] The effective judging circuit 704 judges whether it is satisfied with coincidence of the pattern judging result and the level judging result. That is, in accordance with the pattern with which the sign pattern of continuous "4 Sample" can perform a phase error operation, further, when larger than the threshold as which the signal amplitude was specified beforehand, it judges with it being "effective". When not satisfied with coincidence of two above-mentioned judgments, it judges with it being "invalid", and the judgment signal [""] concerned is supplied to IQ judging circuit 710 as a hold signal.

[0101] Moreover, on the other hand, the phase error arithmetic circuit 701 performs an error operation according to the sign pattern of the absolute-value-ized input signal, and supplies Q error data (error result of an operation

of a Q signal network) which are the result of an operation to the average circuit 707 and a selector 708. And if the average circuit 707 has I error data (error result of an operation of an I signal network) from the phase error arithmetic circuit 1 for I signal networks, it will output this and the averaged result and will give it to a selector 708.

[0102] IQ judging circuit 710 to which the effective judging result of I error data and the effective judging result of Q error data were supplied performs an effective judging, and outputs the switch signal corresponding to the judgment result to a selector 708.

[0103] Namely, the judgment of IQ judging circuit 710 chooses I error data from the phase error arithmetic circuit 1 so that the error data from an I signal may be chosen at the time of "only an I signal is effective." Moreover, the judgment of IQ judging circuit 710 chooses Q error data from the phase error arithmetic circuit 701 so that the error data from a Q signal may be chosen at the time of "only a Q signal is effective." Moreover, in "I signal and a Q signal, the judgment of IQ judging circuit 710 chooses the output of a delay circuit 709 so that the error data in front of 1 clock may be chosen at the time of invalid." The output of the average circuit 707 is chosen so that the error data from an I signal and the data of an average of the error data from a Q signal may be chosen, when the judgment of IQ judging circuit 710 is "effective [both an I signal and a Q signal]." It operates so that it may output to an output terminal 711 by making this into a clock phase error signal.

[0104] The system of an example 3 prepares the error operation and effective judging function the object for I signal networks, and for Q signal networks, respectively. In the average circuit 707 Namely, the error data from an I signal, Take the average of the error data from a Q signal, and it is made to supply a selector 708. The phase error signal delayed one clock also supplies the output of the error data from an I signal, the error data from a Q signal, and a selector 708 to a selector 708. So that it may switch to a selector 708 in IQ judging circuit 710 based on the effective judging result from an I signal, and the effective judging result from a Q signal, and may be made to output a signal and an effective judging may choose the error data from an I signal at the time only of an I signal Moreover, an effective judging so that the error

data from a Q signal may be chosen at the time only of a Q signal Moreover, so that the phase error signal delayed one clock when an I signal and a Q signal were "invalid" may be chosen Moreover, when an I signal and a Q signal are "effective", the average of the error data from an I signal and the error data from a Q signal is chosen, and it was made to output as a clock phase error signal. And this clock phase error signal is used as a phase control signal for correcting the phase shift of a playback clock, phase control of a clock regenerative circuit is carried out, and the phase shift of a playback clock was corrected to the phase control signal correspondence concerned. It becomes possible to raise phase error detection precision further also in a QPSK method by this.

[0105] In addition, as for this invention, it is needless to say that it is not limited to a QPSK method and can apply also to modulation techniques, such as a BPSK method and 8PSK methods.

[0106]

[Effect of the Invention] Since it becomes possible to increase sharply the input configuration in which a phase error operation is possible according to this invention as explained above, clock reproducibility ability is sharply improvable. Therefore, phase error detection can be carried out in a high probability, and the clock phase error detector and the clock phase error detection approach of being able to acquire the clock phase error signal used for the phase correction of a clock regenerative circuit, and having enabled it to satisfy clock reproducibility ability low [C/N] can be offered.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the example of a clock phase error detector configuration as an example of this invention.

[Drawing 2] It is drawing for explaining the example of a setting of the

threshold of the level judging circuit used with this invention equipment.

[Drawing 3] It is the block diagram showing the example of a configuration of the phase error arithmetic circuit used with this invention equipment.

[Drawing 4] It is drawing for explaining the example of the clock phase error detector of this invention of operation.

[Drawing 5] They are the pattern of the input signal of the phase error arithmetic circuit of this invention, and the correspondence Fig. of a filter factor.

[Drawing 6] It is drawing for explaining the pattern of an input signal.

[Drawing 7] It is drawing for explaining conventionally the pattern of the input signal whose clock phase error detection was not completed at all.

[Drawing 8] It is a block diagram explaining other examples of the clock phase error detector of this invention.

[Drawing 9] It is the correspondence Fig. of the input configuration of a phase error arithmetic circuit, and a filter factor in other examples of this invention.

[Drawing 10] It is the block block diagram showing the example of a clock phase error detector of this invention at the time of applying to a rectangular detection output.

[Drawing 11] It is drawing for explaining the conventional technique.

[Drawing 12] It is drawing showing the example of an eye pattern.

[Drawing 13] It is drawing for explaining the conventional technique.

[Drawing 14] It is drawing having shown the conventional clock phase error detection approach typically.

[Drawing 15] It is drawing having shown the conventional clock phase error detection approach typically, and is drawing for explaining the pattern of the input signal which cannot perform clock phase error detection.

[Description of Notations]

1,701 [-- An effective judging circuit, 5 / -- A hold circuit, 501,706 / -- An absolute-value circuit, 707 / -- An average circuit, 708 / -- A selector, 709 / -- A delay circuit, 710 / -- IQ judging circuit.] -- A phase error arithmetic circuit, 2,502,702 -- A pattern judging circuit, 3,703 -- A level judging circuit, 4,704